TECHNICAL PROGRAM

39th International Symposium on Multiple-Valued Logic

May 21-23, 2009

Okinawa Industrial Support Center (Naha, Okinawa, Japan)

IEEE Celebrating 125 Years of Engineering the Future

IEEE computer society

GSIS Graduate School of Information Sciences, TOHOKU University

CERIES

IEEE Fukuoka Section

Wednesday, May 20, 2009

18th International Workshop on Post-Binary ULSI Systems (All Sessions are held in Room 302/303)

10:30-10:35 AM **Opening**

10:35-11:50 AM **Paper Session 1**

Noise-Driven Neural Computing on VLSIs	T. Asai, A. Utagawa (Hokkaido University)
Fuzzy Quantum Circuits to Model Emotional Humanoids	A. Raghuvanshi, M. Perkowski (Portland State University)
Engineering Models and Circuit Realization of Quantum State Machines	M. Kumar, S. Boshra-riad, Y. Nachimuthu, M. A. Perkowski (Portland State University)

11:50AM-1:20 PM **Lunch Break**

1:20-2:35 PM **Paper Session 2**

Reversible Synthesis of Quinary Logic Function	M. H. A. Khan (East West University)
Numeric Function Generators Using Decision Diagrams for Discrete Functions	S. Nagayama, T. Sasao, J. T. Butler (Hiroshima City University)
How to Map Software Loops and Flows into Dibits of Four-Valued Bit Code	C. James III (CEC Services)

2:35-2:50 PM **Break**

2:50-4:05 PM **Paper Session 3**

Analysis of Nurse's Medical Record in The IZANAMI Using Text Mining Method	M. Kushima, K. Araki, M. Suzuki, S. Araki, H. Tamura, K. Tanno, T. Toyama, O. Ishizuka (University of Miyazaki), M. Ikeda (JAIST)
Reed-Muller Adders Based on Binary Stored-Carry-or-Borrow Representation	S. D. Torno(Exorand Technology)
Time and Many-Valuedness: Applications of Three-Valued Temporal Logics	S. Akama(University of Tsukuba)

4:05-4:10 PM **Closing**

5:30-6:00 PM **Registration of ISMVL 2009** (Desk in front of Room 302/303)

6:00 PM **Welcome Party** (Room 302/303)

Thursday, May 21, 2009

9:00-9:10 AM **Opening** (Room 101/102)

9:10-9:50 AM **Invited Talk 1** (Room 101/102)
Counting Problems and Clones of Functions,
Andrei A. Bulatov, Simon Fraser University, Canada

9:50-10:00 AM **Break (10 Minutes)**

10:00:12:05 AM – Session 1A (Room 302/303)

Medical/Health Care Systems Based on Soft Computing

Web-based Nursing Care Quality Improvement System with Fuzzy Recommendation System	R. Sakashita(Hyogo University), A. Uchinuno(University of Hyogo), K. Kamiizumi (Aomori University of Health and Welfare), K. Tei (Aomori University of Health and Welfare), N. Awaya (Oita University)
A Study of Practical Causality Acquisition among Vital Signals	N. Tsuchiya, H. Nakajima (OMRON Corporation)
Biometric System by Foot Pressure Change Based on Neural Network	H. Ye, S. Kobashi, (University of Hyogo) K. Taniguchi(Kinden Corporation) Y. Hata(University of Hyogo), K. Asai(The Kansai Electric Power Co. Inc)
Fuzzy Logic Assisted Quantification of Gyral Deformation Index Using Magnetic Resonance Images for the Infantile Brain	S. Kobashi, Y. Fujimoto (University of Hyogo) M.Ogawa, K. Ando, R. Ishikura (Hyogo College of Medicine), S. Imawaki (Ishikawa Hospital) , S. Hirota (Hyogo College of Medicine), Y. Hata (University of Hyogo)
Fuzzy Rule Extraction from Nursing-care Texts	M. Nii, T. Yamaguchi, Y. Takahashi, A. Uchinuno, R. Sakashita (University of Hyogo)

10:00-12:05 AM – Session 1B (Room 101/102)

Current-Mode Logic

Robust Multiple-Valued Current-Mode Circuit Components Based on Adaptive Reference-Voltage Control	N. Onizawa, T. Hanyu (Tohoku University)
Optimization of Current-Mode MVD-ORNS Arithmetic Circuits	M. Inaba(Tsukuba University of Technology), K. Tanno (University of Miyazaki), R. Sawada (Denso Techno Co), H.Tanaka (Miyakonojo National College of Technology), H. Tamura (University of Miyazaki)
16-Level Current-Mode Multiple-Valued Dynamic Memory with Increased Noise Margin	G. Khodabandehloo, M. Mirhassani, M. Ahmadi (University of Windsor)
Multiple-Valued Reconfigurable VLSI Processor Based on Superposition of Data and Control Signals	N. Okada, M. Kameyama (Tohoku University)
Timing-Variation-Aware Multiple-Valued Current-Mode Circuit for a Low-Power Pipelined System	T. Matsuura, H. Shirahama, M. Natsui, T. Hanyu (Tohoku University)

12:05-1:10 PM **Lunch Break**

1:10-2:50 PM - Session 2A (Room 302/303)

Algebra

Mining Approximative Descriptions of Sets Using Rough Sets	D. A. Simovici, S. Mimaroglu (University of Masschusetts)
Positive Primitive Structures	B. A. Romov (Bayard Rustin Ed Complex)
Paradigms for Non-Classical Substitutions	P. Eklund (Umea University), M.A. Galán (University of Málaga), J. Kortelainen (Mikkeli University of Applied Sciences), L. N. Stout (Illinois Wesleyan University)
Bounding the Phase Transition on Edge Matching Puzzles	C. Mateu, R. Bejar, C. Fernandez, N. Pascual (Universitat de Lleida)

1:10-2:50 PM – Session 2B (Room 101/102)

Quantum Logic

Efficient Implementation of Controlled Operations for Multivalued Quantum Logic	D. Rosenbaum, M. Perkowski (Portland State University)
Quantum Finite State Machines as Sequential Quantum Circuits	M. Lukac, M. Perkowski (Portland State University)
Synthesis of GF(3) Based Reversible/Quantum Logic Circuits Without Garbage Output	A. I. Khan (Univ. of California Berkeley), Md. M. M. Khan, S. Chowdhury, A. K. Biswas, M. Hasan (Bangladesh Univ. of Engineering and Technology)
Quantum Realization of Multiple-Valued Feynman and Toffoli Gates Without Ancilla Input	M. H. A. Khan (East West University)

2:50-3:00 PM **Break (10 Minutes)**

3:00-3:40 PM **Invited Talk 2** (Room 101/102)
Multi-Valued Modal Fixed Point Logics for Model Checking
Koki Nishizawa, Tottori University of Environmental Studies, Japan

3:40-3:50 PM **Break (10 Minutes)**

3:50-5:05 PM – Session 3A (Room 302/303)

Clone Theory 1

Minimal Coverings of Maximal Partial Clones	K. Schölzel (University of Rostock)
Frozen Boolean partial co-clones	G. Nordh (Linköping University,) B. Zanuttini (Universite de Caen Basse-Normandie)
The Minimal Covering of Maximal Partial Clones in 4-Vaued Logic	K. Schölzel (University of Rostock)

3:50-5:30 PM – Session 3B (Room 101/102)

Logic Design and its Application

On the Guidance of Reversible Logic Synthesis by Dynamic Variable Reordering	D. Y. Feinstein (Innoventions, Inc), M. A. Thornton (Southern Methodist University)
Design of a High-Speed Fuzzy Logic Controller Based on Log-Domain Arithmetic	A. Razib, S. Dick, V. Gaudet (University of Alberta)
The Use of Multiple Connected Pseudo Minterms in the Synthesis of MVL Functions	B. A. B. Sarif (KFUPM), M. Abd-El-Barr (Kuwait University)
A Two-Pronged Approach of Power-Aware Voltage Scheduling for Real-Time Task Graphs in Multi-Processor Systems	N. Kamiura, A. Saitoh, T. Isokawa, N. Matsui (University of Hyogo)

Friday, May 22, 2009

9:30-10:10 AM **Invited Talk 3** (Room 101/102)
Computational Neuroscience and Multiple-Valued Logic
Mitsuo Kawato, ATR Computational Neuroscience Laboratories, Japan

10:10-10:20 AM **Break (10 Minutes)**

10:20-11:35 AM –Session 4A (Room 302/303)

Clone Theory 2

Hyperclones Determined by Total Relations	H. Machida (Hitotsubashi University) J. Pantovic (University of Novi Sad)
On Endoprimal Monoids in Clone Theory	H. Machida (Hitotsubasi University), I. G. Rosenberg (University of Montreal)
Partial Clones Containing All Selfdual Monotonic Boolean Partial Functions	L. Haddad (Royal Military College)

10:20-12:00 PM – Session 4B (Room 101/102)

Spectral Logic

On Periodic Patterns and their Spectra	C. Moraga (European Centre for Soft Computing), R. Stankovic (University of Nis), J. T. Astola (Tampere Univ. Technology)
Discrete Hartley Transforms	C. Moraga (European Centre for Soft Computing)
Generating Hard Instances for MaxSAT	J. Planes (Universitat de Lleida), F. Manyà (CSIC) R. Bejar (Universitat de Lleida), A. Cabiscol (UDL)
New Encodings from Max-CSP into Partial Max-SAT	J. Argelich(INESC-ID), A. Cabiscol(UDL), I. Lynce(INESC-ID), F. Manyà(CSIC)

12:00-1:20 PM **Lunch Break**

1:20-2:20 PM **Plenary Session** (Room 101/102)

2:20-5:30 PM **Tour for Okinawa Traditions**

7:00-9:00 PM **Banquet** (at Okinawa Harborview Crowne Plaza)

Saturday, May 23, 2009

9:00-9:40 AM **Invited Talk 4** (Room 101/102)
Multi-Level Signaling for Chip-to-Chip and Backplane Communication (A tutorial)
Ali Sheikholeslami, University of Toronto, Canada

9:40-9:50 AM **Break (10 Minutes)**

9:50-11:55 AM – Session 5A (Room 302/303)

Fuzzy and Rough Sets Theory, and Their Application 1

An Overview of a Software Tool in Rough Non-deterministic Information Analysis	H. Sakai, H. Kimura (Kyushu Institute of Technology), M. Nakata (Josai International University)
On Decision Making under Interval Uncertainty: A New Justification of Hurwicz Optimism-Pessimism Approach and its Use in Group Decision Making	V. N. Huynh, Y. Nakamori (JAIST), C. Hu (University of Central Arkansas), V. Kreinovich (University of Texas at El Paso)
Optimization of Fuzzy if-then Rule Bases by Evolutionary Tuning of the Operations	C. Moraga (European Centre for Soft Computing), M. Sugeno (Doshisha University) , E. Trillas (European Centre for Soft Computing)
Non-Convex Fuzzy Truth Values and De Morgan Bisemilattices	N. Takagi(Toyama Prefectural University)
Evaluation of the Hierarchical Temporal Memory as Soft Computing Platform and Its VLSI Architecture	W. J.C.Melis, S. Chizuwa, M. Kameyama (Tohoku University)

9:50-11:55 AM – Session 5B (Room 101/102)

Multiple-Valued VLSI

Multiple-Valued Constant-Power Adder for Cryptographic Processors	Y. Baba, A. Miyamoto, N. Homma, T. Aoki (Tohoku University)
Time-Interleaved Polyphase Decimation Filter Using Signed-Digit Adders	M. Murozuka, K. Ikeura, F. Adachi, K. Machida, T. Waho (Sophia University)
Multiple-Valued Data Transmission Based on Time-Domain Pre-Emphasis Techniques in Consideration of Higher-Order Channel Effects	Y. Yuminaka, Y. Takahashi, K. Henmi (Gunma University)
Quaternary Addition Circuits Based on SUSLOC Voltage-Mode Cells and Modeling with SystemVerilog	M. A. Thornton (Southern Methodist University), S. R. Datla (Texas Instruments), L. Hendrix, D. Henderson (Omnibase Logic)
Multiple Valued Logic Algebra for the Synthesis of Digital Circuits	M. E. R. Romero, E. M. Martins (Federal University of Mato Grosso do Sul), R. R. Santos (Dom Bosco Catholic University)

11:55-1:00 PM **Lunch Break**

1:00-1:40 PM **Invited Talk 5** (Room 101/102)
Designing and Using FPGAs Beyond Classical Binary Logic: Opportunities in Nano-scale Integration Age
Zeljko Zilic, McGill University, Canada

1:40-1:50 PM **Break (10 Minutes)**

1:50-3:30 PM - Session 6A (Room 302/303)

Fuzzy and Rough Sets Theory, and Their Application 2

Attribute Reduction as Calculation of Focus in Granular Reasoning	Y. Kudo (Muroran Institute of Technology) , T. Murai (Hokkaido University)
Clarifying the Systems of Axioms Based on the Method of Indeterminate Coefficients	T. Ninomiya (Tamagawa University), M. Mukaidono (Meiji University)
Applying Rough Sets to Information Tables Containing Missing Values	M. Nakata (Josai International University), H. Sakai (Kyushu Institute of Technology)
Generalized Extended t-Norms as t-Norms of Type 2	M. F. Kawaguchi, M. Miyakoshi (Hokkaido University)

1:50-3:30 PM – Session 6B (Room 101/102)

Logic Design

Evaluation of Cardinality Constraints on SMT-based Debugging	A. Suelflow, R. Wille, G. Fey, R. Drechsler (University of Bremen)
Application of Covering Codes for Reduced Representation of Logic Functions	J. T. Astola (Tampere University of Technology), R. S. Stankovic (University of Nis)
Ternary Logic by 3rd Subharmonics and its Application to Multiway Switches	T. Soma (Illinois College), T. Soma
Fixed Polarity Quaternary Transforms Derived from Linearly Independent Transform over GF(2) Structurev	B. J. Falkowski, C. C. Lozano (NTU), T. Luba (Warsaw University of Technology)

3:30-3:40 PM **Break (10 Minutes)**

3:40-5:20 PM – Session 7A (Room 302/303)

Emerging Device

Equivalence Checking of Reversible Circuits	R. Wille, D. Große (University of Bremen), D. M. Miller (University of Victoria), R. Drechsler (University of Bremen)
Multi-Path Switching Device Utilizing A Multi-Terminal Nanowire Junction for MDD-Based Logic Circuit	S. Kasai, Y. Shiratori, K. Miura (Hokkaido University), N. Wu (Chinese Academy of Sciences)
Multiple-valued Logic Gates Using Asymmetric Single-Electron Transistors	W. Zhang, N. Wu (Chinese Academy of Sciences), S. Kasai, T. Hashizume (Hokkaido University)
Scalable Architectures for Synthesis of Reversible Quaternary Multiplexer and Demultiplexer Circuits	M. H. A. Khan (East West University)

3:40-5:20 PM – Session 7B (Room 101/102)

Decision Diagrams and Reed-Muller Expansion

Floating-Point Numerical Function Generators Using EVMDDs for Monotone Elementary Functions	S. Nagayama (Hiroshima City University), T. Sasao (Kyushu Institute of Technology), J. T. Butler (Naval Postgraduate School)
Representing the Genetic Code as a Function on a Galois Field Using the Reed-Muller Expansion	H. A. Aleem, D. H. Green, F. Mavituna (University of Manchester)
A Quaternary Decision Diagram Machine and the Optimization of its Code	T Sasao, H. Nakahara, M. Matsuura (Kyushu Institute of Technology), Y. Kawamura (Renesas Technology), J. T. Butler (Naval Postgraduate School)
Quaternary Reed-Muller Expansions of Mixed Radix Arguments in Cryptographic Circuits	A. Rafiev, J. P. Murphy, A. Yakovlev (Newcastle University)

5:20-5:30 PM **Closing** (Room 101/102)