46th IEEE International Symposium on Multiple-Valued Logic

ISMVL 2016

May 18 – 20, 2016, Hokkaido University, Sapporo, Japan

Final Program

Sponsored by:

IEEE Computer Society

TC on Multiple-Valued Logic

Japan Research Group of MVL

National Institute of Information and Communications Technology

May 17, Tuesday		
10:00	Post-Binary ULSI Workshop Workshop Chair: *H. Nakahara*	**Room: Seminar Room 1**
18:00	ISMVL Welcome Reception (ULSI WS Student Poster Session)	**Kogakubu Syokudo (Cafeteria)**

May 18, Wednesday		
09:00	Opening Symposium Chair: *T. Hanyu* and Program Chair: *Y. Yuminaka*	**Room: Akira Suzuki Hall (ASH)**
09:15	**[Keynote Address I]** Chair: *T. Hanyu* **Elucidation of Brain Activities by Electroencephalograms and its Application to Brain Computer Interface** *Takahiro Yamanoi (Hokkai-Gakuen University, Japan)*	**Room: ASH**
10:00	Coffee/Tea Break	**Entrance Hall**
	[Session 1A: Circuits I] Chair: *M. Natsui* **Room: ASH**	**[Session 1B: Synthesis of Reversible Circuits]** Chair: *R. Wille* **Room: Seminar Room 2 (SR2)**
10:20	**Energy-Efficient and Highly-Reliable Nonvolatile FPGA Using Self-Terminated Power-Gating Scheme** *D. Suzuki and T. Hanyu*	**Re-writing HDL Descriptions for Line-aware Synthesis of Reversible Circuits** *Z. Alwardi, R. Wille, and R. Drechsler*
10:45	**CNTFET-RFB: An Error Correction Implementation For Multi-Valued CNTFET Logic** *G. Sundararajan and C. Winstead*	**An Improved Factorization Approach to Reversible Circuit Synthesis Based on EXORs of Products of EXORs** *L. Tran, A. Gronquist, M. Perkowski, and J. Caughman*
11:10	**Ternary versus Binary Multiplication with Current-Mode CNTFET-based K-Valued Converters** *M. Moradi, R. F. Mirzaee, and K. Navi*	**Fault Detection in Parity Preserving Reversible Circuits** *N. Przigoda, G. Dueck, R. Wille, and R. Drechsler*
11:35	**Design of Ratioless Ternary Inverter using Graphene Barristor** *C.-H. Shim, S. Heo, J. Noh, Y. J. Kim, S.-Y. Kim, A. K. Khan, and B. H. Lee*	**Notes on Majority Boolean Algebra** *A. Chattopadhyay, L. Amaru, M. Soeken, P.-E. Gaillardon, and G. De Micheli*
12:00	Lunch (Symposium Subcommittee Meeting)	**Hokubu Shokudo (Cafeteria)**

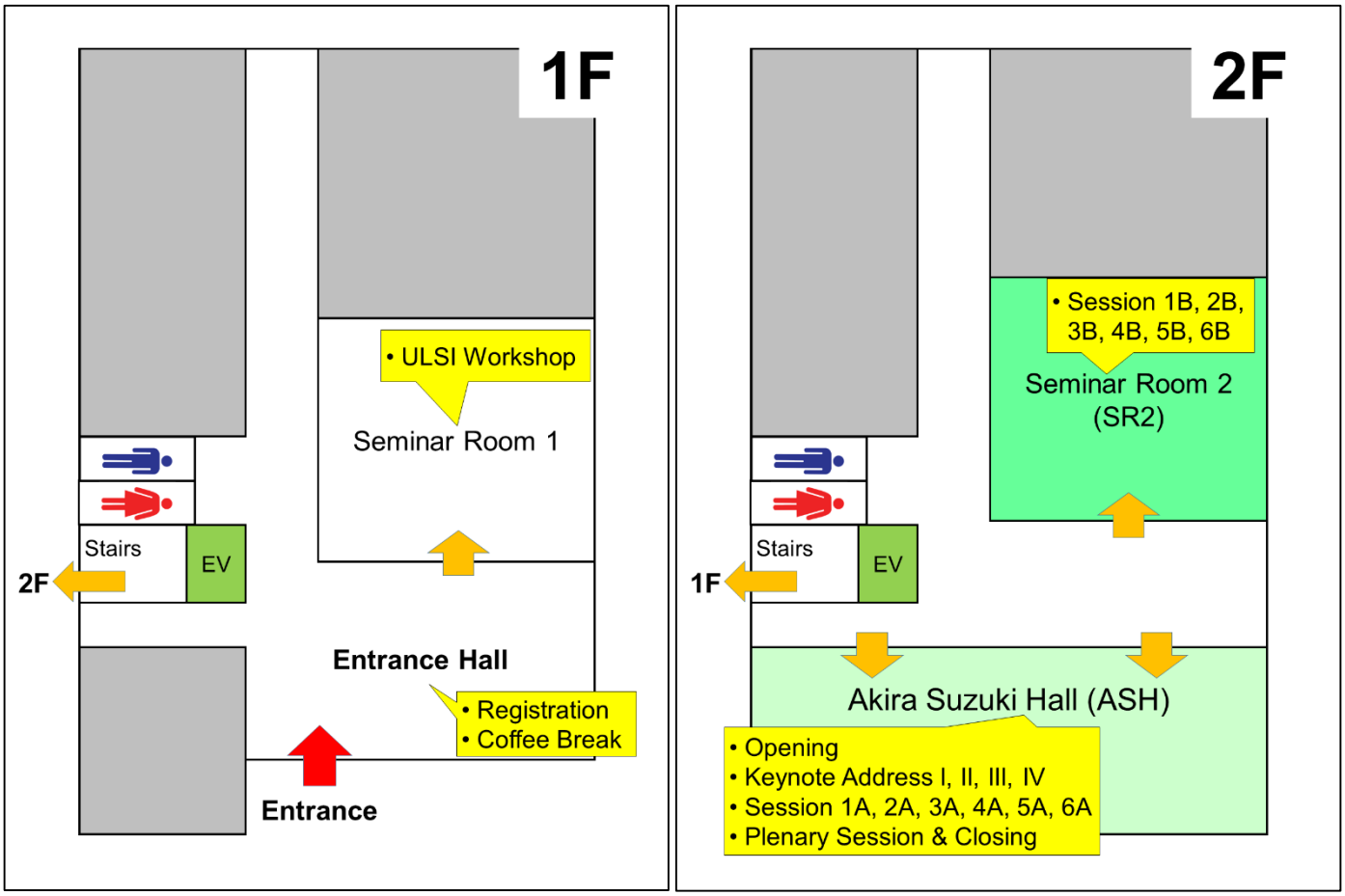
May 18, Wednesday (continued)		
13:20	**[Keynote Address II]** Chair: *M. F. Kawaguchi* **Room: ASH** **Realization of Associative Image Search: Development of Image Retrieval Platform for Enhancing Serendipity** *Miki Haseyama (Hokkaido University, Japan)*	
14:05	Coffee/Tea Break **Entrance Hall**	
	[Session 2A: Circuits II] Chair: *N. Homma* **Room: ASH**	**[Session 2B: Clone]** Chair: *D. Simovici* **Room: SR2**
14:20	**An FFT Circuit Using Nested RNS in a Digital Spectrometer for a Radio Telescope** *H. Nakahara, T. Sasao, H. Nakanishi, K. Iwai, T. Nagao, and N. Ogawa*	**Monomial Clones: Local Results and Global Properties** *H. Machida and J. Pantovic*
14:45	**Double-Rate Equalization Using Tomlinson-Harashima Precoding for Multi-Valued Data Transmission** *Y. Iijima and Y. Yuminaka*	**Centralizing Monoids on a Three-Element Set Related to Binary Idempotent Functions** *H. Machida and I. G. Rosenberg*
15:10	**Context-Based Error Correction Scheme Using Recurrent Neural Network for Resilient and Efficient Intra-Chip Data Transmission** *N. Sugaya, M. Natsui, and T. Hanyu*	**Minimal Weighted Clones with Boolean Support** *P. G. Jeavons, A. Vaicenavicius, and S. Zivny*
15:35	Coffee/Tea Break **Entrance Hall**	
	[Session 3A: Index Generation Functions] Chair: *Y. Iguchi* **Room: ASH**	**[Session 3B: Algebra I]** Chair: *F. Manya* **Room: SR2**
15:50	**An Efficient Heuristic for Linear Decomposition of Index Generation Functions** *S. Nagayama, T. Sasao, and J. T. Butler*	**Set Representation of Partial Dynamic De Morgan Algebras** *I. Chajda and J. Paseka*
16:15	**Index Generation Functions based on Linear and Polynomial Transformations** *H. Astola, R. Stankovic, and J. Astola*	**Tolerance Distances on Minimal Coverings** *C. Zara and D. A. Simovici*
16:40	**An Algebraic Approach to Reducing the Number of Variables of Incompletely Defined Discrete Functions** *J. Astola, P. Astola, R. Stankovic, and I. Tabus*	**Paraconsistent Double Negation That Can Simulate Classical Negation** *Norihiro Kamide*
17:05	**A Realization of Index Generation Functions Using Multiple IGUs** *T. Sasao*	**Cut-Free Systems for Restricted Bi-Intuitionistic Logic and Its Connexive Extension** *Norihiro Kamide*

May 19, Thursday		
09:15	**[Keynote Address III]** Chair: *T. Sasao* **Room: ASH** **Power of Enumeration --- BDD/ZDD-Based Techniques for Discrete Structure Manipulation** *Shin-ichi Minato (Hokkaido University, Japan)*	
10:00	Coffee/Tea Break **Entrance Hall**	
	[Session 4A: From Reversible to Quantum Circuits] Chair: *M. Lukac* **Room: ASH**	**[Session 4B: Algebra II]** Chair: *J. Paseka* **Room: SR2**
10:20	**Integrated Synthesis of Linear Nearest Neighbor Ancilla-Free MCT Circuits** *M. M. Rahman, G. W. Dueck, A. Chattopadhyay, and R. Wille*	**Some Properties of Generalized State Operators on Residuated Lattices** *M. Kondo and M. F. Kawaguchi*
10:45	**Technology Mapping of Reversible Circuits to Clifford+T Quantum Circuits** *N. Abdessaied, M. Amy, M. Soeken, and R. Drechsler*	**Simple Characterizations of Perfect Residuated Lattices** *M. Kondo*

May 19, Thursday (continued)		
11:10	**Nearest-Neighbor and Fault-Tolerant Quantum Circuit Implementation** *L. Biswal, C. Bandyopadhyay, A. Chattopadhyay, R. Wille, R. Drechsler, and H. Rahaman*	
11:40	Lunch, Excursion to NIKKA WHISKY & Otaru Canal, and Banquet at Keio Plaza Hotel Sapporo	

May 20, Friday		
09:15	**[Keynote Address IV]** Chair: *Y. Yuminaka* **Room: ASH** **SPRUCE, an Embedded Compact Stack Machine for IGBT Power Modules** *Wai Tung Ng and Andrew Shorten (University of Toronto, Canada)*	
10:00	Coffee/Tea Break **Entrance Hall**	
	[Session 5A: Intelligent Medical and Welfare Engineering] Chair: *T. Araki* **Room: ASH**	**[Session 5B: Logic I]** Chair: *S. Nagayama* **Room: SR2**
10:15	**Gray-Scale Morphology Based Image Segmentation and Character Extraction Using SVM** *J. Chen and N. Takagi*	**Gibbs Characterization of Binary and Ternary Bent Functions** *R. S. Stankovic, M. Stankovic, J. T. Astola, and C. Moraga*
10:40	**A Low-Voltage and Low-Power CMOS Temperature Sensor Circuit with Digital Output for Wireless Healthcare Monitoring System** *A. Setiabudi, R. Sakamoto, H. Tamura, and K. Tanno*	**On Constructing Secure and Hardware-Efficient Invertible Mappings** *E. Dubrova*
11:05	**Dependency Analysis of BMI in Health Checkup Blood Data** *M. Higuchi, K. Sorachi, and Y. Hata*	**Formal Design of Pipelined GF Arithmetic Circuits and Its Application to Cryptographic Processors** *R. Ueno, Y. Sugawara, N. Homma, and T. Aoki*
11:30	**Novel Instrumentation Amplifier Architectures Insensitive to Resistor Mismatches and Offset Voltage for Biological Signal Processing** *Z. Abidin, K. Tanno, S. Mago, and H. Tamura*	**Realization of FIR Digital Filters Based on Stochastic/Binary Hybrid Computation** *S. Koshita, N. Onizawa, M. Abe, T. Hanyu, and M. Kawamata*
11:55	**Study Support System of Character Drawing considering Feeling Evaluation** *R. Murakami and N. Muranaka*	**The Pascal triangle (1654), the Reed-Muller-Fourier Transform (1992), and the Discrete Pascal Transform (2005)** *C. Moraga, R. Stankovic, and M. Stankovic*
12:20	Lunch (Executive Subcommittee Meeting) **Hokubu Shokudo (Cafeteria)**	
	[Session 6A: Quantum Gates and Quantum States] Chair: *G. Dueck* **Room: ASH**	**[Session 6B: Logic II]** Chair: *R. Stankovic* **Room: SR2**
13:40	**New Two-Qubit Gate Library with Entanglement** *M. B. Ali, T. Hirayama, K. Yamanaka, and Y. Nishitani*	**A Study on Realizing Awareness Using 3VL-MLP** *Q. Zhao*
14:05	**Quantum p-Valued Toffoli and Deutsch Gates with Conjunctive or Disjunctive Mixed Polarity Control** *C. Moraga*	**Multi-Valued Problem Solvers** *B. Steinbach, S. Heinrich, and C. Posthoff*
14:30	**Logic Synthesis for Quantum State Generation** *P. Niemann, R. Datta, and R. Wille*	**A Bit-Vector Approach to Satisfiability Testing in Finitely-Valued Logics** *J. R. Soler and F. Manya*
14:55	**Quantum Algorithmic Complexity of Three-Qubit Pure States** *M. Lukac and A. Mandilara*	**On the Inadmissible Class of Multiple-Valued Faulty-Functions under Stuck-at Faults** *D. Chowdhury, D. K. Das, B. B. Bhattacharya, and T. Sasao*
15:20	Coffee/Tea Break **Entrance Hall**	
15:30	Plenary Session and Closing **Room: ASH**	

Brief Map of the Building



Brief Map for Reception & Lunch (Outside the Building)