

ISMVL-2013
IEEE 43rd International Symposium on Multiple-Valued Logic
Toyama International Conference Center, Toyama, Japan, May 21 – 24



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IEEE Computer Society



TC on Multiple-Valued Logic



Japan MVL Research Group

FINAL PROGRAM

May 21, Tuesday

09:00	Post-Binary ULSI Workshop Registration	2F Foyer
09:40	[Post-Binary ULSI Workshop Invited Talk] Ultrahigh-Speed Digital-to-Analog Converters for Multi-Level Optical Transmission Systems <i>Munehiko Nagatani, Hideyuki Nosaka, Shogo Yamanaka, and Koichi Murata (NTT Photonics Lab., Japan)</i>	Room 201
10:55	Post-Binary ULSI Workshop Regular Sessions Workshop Co-Chairs: N. Homma and S. Nagayama	Room 201
17:00	ISMVL Registration	2F Foyer
18:00	ISMVL Welcome Reception (ULSI WS Student Poster Session)	3F Foyer

May 22, Wednesday

08:15	ISMVL Registration	2F Foyer
08:45	Opening Symposium Chair: T. Waho and Program Chair: Y. Yuminaka	Room 201/202
09:00	[Invited Address I] Chair: T. Waho Computational Medical and Health Care Technology <i>Yutaka Hata (University of Hyogo, Japan) and Hiroshi Nakajima (Omron Co., Japan)</i>	Room 201/202
09:50	Break	
	[Session 1A: Medical and Health Care Engineering] Chair: N. Kamiura Room 201/202	[Session 1B: Reversible Circuits] Chair: M. Lukac Room 203
10:10	Systems Health Care – Health Management Technology – <i>H. Nakajima, T. Shiga, and Y. Hata</i>	Fault Ordering for Automatic Test Pattern Generation of Reversible Circuits <i>R. Wille, H. Zhang, and R. Drechsler</i>
10:35	Wearable Human Activity Recognition by Electrocardiograph and Accelerometer <i>T. Fujimoto, H. Nakajima, N. Tsuchiya, H. Marukawa, K. Kuramoto, S. Kobashi, and Y. Hata</i>	Synthesis of Reversible Circuits Based on Exclusive OR Sums <i>B. Schaeffer, L. Tran, A. Gronquist, M. Perkowski, and P. Kerntopf</i>
11:00	Gaze Estimation Using Electrooculogram Signals and Its Mathematical Modeling <i>M. Yan, H. Tamura, and K. Tanno</i>	Multiple-Valued Reversible Benchmarks and Extensible Quantum Specification (XQS) Format <i>M. Hawash, M. Lukac, M. Kameyama, and M. Perkowski</i>
11:25	Fuzzy Damage Extraction Method for Ultrasonic Nondestructive Testing Images <i>K. Tsukuda, T. Egawa, K. Taniguchi, K. Kuramoto, S. Kobashi, and Y. Hata</i>	Analysis and Improvement of Transformation-Based Reversible Logic Synthesis <i>C. Chandak, A. Chattopadhyay, S. Majumder, and S. Maitra</i>
11:50	Lunch (Symposium Committee)	

May 22, Wednesday (continued)		
	[Session 2A: Medical and Wellness Applications] Chair: <i>H. Nakajima</i> Room 201/202	[Session 2B: Logic Design/Switching Theory I] Chair: <i>E. Dubrova</i> Room 203
13:00	A Fuzzy Human Detection for Security System Using Infrared Laser Camera <i>T. Takeda, K. Kuramoto, S. Kobashi, and Y. Hata</i>	Remarks on Applications of Shapes of Decision Diagrams in Classification of Multiple-Valued Logic Functions <i>S. Stanković, R. S. Stanković, and J. Astola</i>
13:25	Mining Multi Human Locations Using Thermopile Array Sensors <i>M. Kuki, H. Nakajima, N. Tsuchiya, K. Kuramoto, S. Kobashi, and Y. Hata</i>	A Machine to Evaluate Decomposed Multi-Terminal Multi-Valued Decision Diagrams for Characteristic Functions <i>H. Nakahara, T. Sasao, and M. Matsuura</i>
13:50	On Selection of Intraocular Power Formula Using Support Vector Machines and Genetic Algorithm <i>N. Kamiura, T. Fukuda, A. Saitoh, T. Isokawa, N. Matsui, and H. Tabuchi</i>	An Application of Autocorrelation Functions to Find Linear Decompositions for Incompletely Specified Index Generation Functions <i>T. Sasao</i>
14:15	A Broken Line Classification Method of Mathematical Graphs for Automating Translation into Scalable Vector Graphic <i>N. Takagi and J. Chen</i>	A Transfer Function Model for Ternary Switching Logic <i>M. A. Thornton</i>
14:40	On Synthesis and Verification from Event Diagrams in a Robot Theatre Application <i>M. Perkowski, A. Bhutada, M. Lukac, and M. Sunardi</i>	Spectral Response of Ternary Logic Netlists <i>M. A. Thornton and T. W. Manikas</i>
15:05	Break	
	[Session 3A: Clone Theory I] Chair: <i>A. Bulatov</i> Room 201/202	[Session 3B: Circuits I] Chair: <i>K. Tanno</i> Room 203
15:20	A Study on Essentially Minimal Clones <i>H. Machida and I. G. Rosenberg</i>	Design and Evaluation of a Differential Switching Gate for Low-Voltage Applications <i>M. Natsui, K. Kashiuchi, and T. Hanyu</i>
15:45	A Solution to a Problem of D. Lau: Complete Classification of Intervals in the Lattice of Partial Boolean Clones <i>M. Couceiro, L. Haddad, K. Schölzel, and T. Waldhauser</i>	A Successive Approximation A/D Converter Using Generalized Non-Binary Algorithm <i>Y. Kurisu, T. Sasaki, and T. Waho</i>
16:10	On the Clones Containing a Near-Unanimity Function <i>D. Zhuk and S. Moiseev</i>	A Graph-Based Approach to Designing Parallel Multipliers over Galois Fields Based on Normal Basis Representations <i>K. Okamoto, N. Homma, and T. Aoki</i>
16:35	Intersections with Ślupecki Partial Clones on a Finite Set <i>L. Haddad and K. Schölzel</i>	Low-Power Multiple-Valued Source-Coupled Logic Circuits Using Dual-Supply Voltages for a Reconfigurable VLSI <i>X. Bai and M. Kameyama</i>
17:00	Not Finitely Definable Partial Clones on a Finite Set <i>B. A. Romov</i>	Dramatically Low-Transistor-Count High-Speed Ternary Adders <i>R. F. Mirzaee, M. H. Moaiyeri, M. Maleknejad, K. Navi, and O. Hashemipour</i>

May 23, Thursday		
08:45	[Invited Address II] Chair: <i>H. Machida</i> The Complexity of Łukasiewicz Logic <i>Martin Goldstern (Vienna University of Technology, Austria)</i>	Room 201/202
9:35	Break	
	[Session 4A: Clone Theory II] Chair: <i>M. Courceiro</i> Room 201/202	[Session 4B: Algebra and Logic I] Chair: <i>N. Takagi</i> Room 203
9:50	On Hyper Co-Clones <i>J. Čolić, H. Machida, and J. Pantović</i>	Four Decades of Multi-Valued Logic: Lists of Highly Cited Papers <i>T. Sasao</i>
10:15	Clones of Partial Cofunctions <i>S. Kerkhoff and F. M. Schneider</i>	Chaotic Time Series Prediction Using Neuro-Fuzzy Systems with Cluster-Based Tribes Optimization Algorithm <i>C.-H. Chen, R.-Z. Jhang, and Y.-Y. Liao</i>
10:40	Boolean Max-Co-Clones <i>A. A. Bulatov</i>	Join Operations on Commutative BCK-Algebras with Condition (S) <i>M. F. Kawaguchi, K. Minami, and M. Kondo</i>
11:10	[Special Talk] Chair: <i>K. Nakashima</i> Local Energy Production for Local Consumption Using Micro Hydro Power <i>Hiroyuki Uesaka (Toyama University of International Studies, Japan)</i>	Room 201/202
12:00	Excursion to Gokayama / Zuiryu-ji with lunch	
19:00	Banquet	

May 24, Friday		
08:45	[Invited Address III] Chair: <i>Y. Yuminaka</i> Highly Reliable Non-Volatile Logic Circuit Technology and Its Application <i>H. Kimura, Z. Zhong, Y. Mizuochi, N. Kinouchi, Y. Ichida, and Y. Fujimori (Rohm Co., Ltd., Japan)</i>	Room 201/202
09:35	Break	
	[Session 5A: Algebra and Logic II] Chair: <i>T. Araki</i> Room 201/202	[Session 5B: Circuits II] Chair: <i>M. Natsui</i> Room 203
09:50	Tense Operators and Dynamic De Morgan Algebra <i>I. Chajda and J. Paseka</i>	Comparing Performance of a Multiple-Valued Time-Based Serial Data Link with Other Serial Links <i>M. Rashdan and J. Haslett</i>
10:15	On the Combinatorics of Tolerance Relations <i>D. A. Simovici</i>	Lowering Error Floors in Stochastic Decoding of LDPC Codes Based on Wire-Delay Dependent Asynchronous Updating <i>N. Onizawa, W. Gross, T. Hanyu, and V. Gaudet</i>
10:40	On Natural Eight-Valued Reasoning <i>N. Kamide</i>	Expandable MVL Inverter Compatible with Standard CMOS Process and Its Application to MVL Hysteresis Comparator <i>A. A. Mannan, K. Tanno, H. Tamura, T. Toyama, and A. Darmawansyah</i>
11:05	Embedding-Based Methods for Trilattice Logic <i>N. Kamide</i>	Accurate and High-Speed Asynchronous Network-on-Chip Simulation Using Physical Wire-Delay Information <i>T. Hanyu, Y. Watanabe, and A. Matsumoto</i>
11:30	On the Semigroup of Equational Classes of Finite Functions <i>J. Almeida, M. Courceiro, and T. Waldhauser</i>	An Area-Efficient Multiple-Valued Reconfigurable VLSI Architecture Using an X-Net <i>X. Bai and M. Kameyama</i>
11:55	Lunch (Executive Committee)	

May 24, Friday (continued)		
	[Session 6A: Logic Design/Switching Theory II] Chair: M. Miller Room 201/202	[Session 6B: Algebra and Reversible Circuits] Chair: G. Dueck Room 203
13:20	Noise-Tolerant Model of a Ternary Inverter Based on Markov Random Field <i>G. Tangim, S. Yanushkevich, S. Kasai, and V. Shmerko</i>	Debugging of Reversible Circuits Using πDDs <i>L. Tague, M. Soeken, S. Minato, and R. Drechsler</i>
13:45	Minimization of the Number of Edges in an EVMDD by Variable Grouping for Fast Analysis of Multi-State Systems <i>S. Nagayama, T. Sasao, and J. T. Butler</i>	Analysis of Reversible and Quantum Finite State Machines Using Homing, Synchronizing and Distinguishing Input Sequences <i>M. Lukac, M. Kameyama, M. Perkowski, and P. Kerntopf</i>
14:10	Secure Key Storage Using State Machines <i>N. Li, S. S. Mansouri, and E. Dubrova</i>	Exact Template Matching Using Boolean Satisfiability <i>N. Abdessaied, M. Soeken, R. Wille, and R. Drechsler</i>
14:35	The Impact of Address Arithmetic on the GPU Implementation of Fast Algorithms for the Vilenkin-Chrestenson Transform <i>D. Gajić and R. S. Stanković</i>	Synthesis of Balanced Ternary Reversible Logic Circuit <i>B. Mondal, P. Sarkar, P. K. Saha, and S. Chakraborty</i>
15:00	Solution of the Last Open Four-Colored Rectangle-Free Grid – An Extremely Complex Multiple-Valued Problem <i>B. Steinbach and C. Posthoff</i>	Contribution to the Study of Multiple-Valued Bent Functions <i>C. Moraga, M. Stanković, R. S. Stanković, and S. Stojković</i>
15:25	Ternary Logic Network Justification Using Transfer Matrices <i>M. A. Thornton and J. L. Dworak</i>	Alternative Proof of Mulholland's Theorem and New Solutions to Mulholland Inequality <i>M. Petrik, M. Navara, and P. Sarkoci</i>
15:50	Break	
16:00	Plenary Session	Room 201/202
17:00	Closing Symposium Chair: T. Waho	Room 201/202
17:00	Reed-Muller Workshop Registration	2F Foyer
17:40	[Reed-Muller Workshop Invited Talk (Open for ISMVL Attendees)] Recent Topics on BDD/ZBDD-Based Discrete Structure Manipulation <i>Shin-ichi Minato (Hokkaido University, Japan)</i>	Room 201
19:30	Reed-Muller Workshop Workshop Chair: T. Sasao	Room 201

May 25, Saturday		
		Room 201
8:45	Reed-Muller Workshop Workshop Chair: T. Sasao	

Sessions marked with * are open to the public.

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