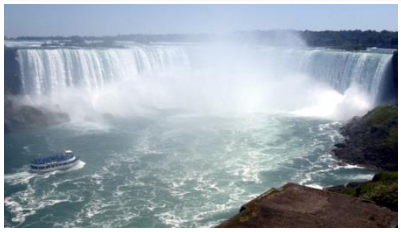
45th IEEE International Symposium on Multiple-Valued Logic

ISMVL 2015

May 18 – 20, 2015, University of Waterloo, Ontario, Canada

Preliminary Program

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TC on Multiple-Valued Logic

UNIVERSITY OF WATERLOO — University of Waterloo

May 17, Sunday	
	Post-Binary ULSI Workshop Workshop Chair: *H. Nakahara*
	ISMVL Welcome Reception

May 18, Monday		
08:00	ISMVL Registration Desk Open	
08:45	Opening Symposium Chair: *V. Gaudet* and Program Chair: G. *Dueck*	
09:00	**[Keynote Address I]** Chair: *L. Haddad* **Algebras and Algorithms** *Matt Valeriote (McMaster University, Canada)*	
10:00	Coffee/Tea Break	
	[Session 1A: Reversible Logic I] Chair: *M. Soeken*	**[Session 1B: Algebra I]** Chair: *M. Couceiro*
10:30	**Reversible Logic Synthesis via Biconditional Binary Decision Diagrams** *A. Chattopadhyay, A. Littarru, L. Amarú, P.-E. Gaillardon, and G. De Micheli*	**Quotient Structures of Non-Commutative Residuated Lattices** *M. Kondo*
11:00	**Online Testing for Three Fault Models in Reversible Circuits** *M. A. Nashiry, G. G. Bhasker, and J. E. Rice*	**Cut-Down Operations on Bilattices** *T. M. Ferguson*
11:30	**An Efficient Reduction of Common Control Lines for Reversible Circuit Optimization** *A. Deb, R. Wille, R. Drechsler, and D. K. Das*	**Finding Hard Instances of Satisfiability in Łukasiewicz Logics** *M. Bofill, F. Manyà, A. Vidal, and M. Villaret*
12:00	Lunch (Symposium Subcommittee Meeting)	
	[Session 2A: Quantum Computing] Chair: *C. Moraga*	**[Session 2B: Circuits over Galois Fields]** Chair: *T. Waho*
13:30	**Design of a Compact Ternary Parallel Adder/Subtractor Circuit in Quantum Computing** *N. J. Lisa and H. M. H. Babu*	**Formal Design of Galois-Field Arithmetic Circuits Based on Polynomial Ring Representation** *R. Ueno, N. Homma,Y. Sugawara, and T. Aoki*
14:00	**An Examination of the NCV-|v1> Quantum Library Based on Minimal Circuits** *A. A.-Abhari, R. Wille, R. Drechsler*	**System for Automatic Generation of Parallel Multipliers over Galois Fields** *Y. Sugawara, R. Ueno, N. Homma, and T. Aoki*
14:30	Coffee/Tea Break	

May 18, Monday (continued)		
	[Session 3A: Reversible Logic II] Chair: *J. Rice*	**[Session 3B: Algebra II]** Chair: *H. Machida*
10:30	**Fredkin-Enabled Transformation-Based Reversible Logic Synthesis** *M. Soeken and A. Chattopadhyay*	**Standard Completeness for Uninorm-Based Logics** *P. Baldi and A. Ciabattoni*
11:00	**Single-Electron Transistor Based Implementation of NOT, Feynman, and Toffoli Gates** *M. H A Khan*	**Hereditarily Rigid Relations** *M. Couceiro, L. Haddad, M. Pouzet, and K. Schölzel*
11:30	**Dynamic Template Matching with Mixed-Polarity Toffoli Gates** *M. M. Rahman, M. Soeken, and G. W. Dueck*	**Valuations in Nilpotent Minimum Logic** *P. Codara and D. Valota*

May 19, Tuesday		
09:00	**[Keynote Address II]** Chair: *D. M. Miller* **Contextuality Supplies the Magic for Quantum Computation** *Mark Howard, Joel Wallman (University of Waterloo, Canada), Victor Veitch (University of Toront, Canada), and Joseph Emerson (University of Waterloo, Canada)*	
10:00	Coffee/Tea Break	
	[Session 4A: Application-Specific Circuits] Chair: *R. S. Stanković*	**[Session 4B: Data Mining]** Chair: *B. Steinbach*
10:30	**An RNS FFT Circuit Using LUT Cascades Based on a Modulo EVMDD** *H. Nakahara, T. Sasao, H. Nakanishi, and K. Iwai*	**A Novel Weighted Hierarchical Adaptive Voting Ensemble Machine Learning Method for Breast Cancer Detection** *C. Deng and M. Perkowski*
11:00	**Non-Binary Analog-to-Digital Converter Based on Amoeba-Inspired Neural Network** *U. Ishida, Y. Yamazaki, and T. Waho*	**Computation Time Reduction to Speed-up the Database Searching Process** *T. Bonny and B. Soudan*
11:30	**Early-Stage Operation-Skipping Scheme for Low-Power Stochastic Image Processors** *D. Katagiri, N. Onizawa, and T. Hanyu*	**Grading Evaluation Method in Character Drawing Study Support System** *R. Murakami and N. Muranaka*
12:00	Lunch, Excursion to Niagara Falls, and Banquet at Rockway Vineyards	

May 20, Wednesday		
09:00	**[Keynote Address III]** Chair: *T. Hanyu* **Novel VLSI Architectures for Real-World Intelligent Systems** *Michitaka Kameyama (Tohoku University, Japan)*	
10:00	Coffee/Tea Break	
	[Session 5A: Logic and Stateflow Models] Chair: *T. Sasao*	**[Session 5B: Memory Circuits]** Chair: *V. Gaudet*
10:30	**Contribution to the Study of Ternary Functions with a Bent Reed-Muller Spectrum** *C. Moraga, M. Stanković, and R. S. Stanković*	**Write-Operation Frequency Reduction for Nonvolatile Logic LSI with a Short Break-Even Time** *T. Akutsu, M. Natsui, and T. Hanyu*
11:00	**Towards Fuzzy Partial Logic** *L. Běhounek and V. Novák*	**A Multi-Level Cell for STT-MRAM with Biaxial Magnetic Tunnel Junction** *A. Vatankhahghadim and A. Sheikholeslami*
11:30	**Using SPIN to Check Nondeterministic Simulink Stateflow Models** *C. Yamada and D. M. Miller*	
12:00	Lunch (Executive Subcommittee Meeting)	

May 20, Wednesday (continued)		
	[Session 6A: Decision Diagrams] Chair: *R. Wille*	**[Session 6B: Clones]** Chair: *F. Manyà*
13:30	**A Reduction Method for the Number of Variables to Represent Index Generation Functions: s-Min Method** *T. Sasao*	**Bounded Bases of Strong Partial Clones** *V. Lagerkvist, M. Wahlström, and B. Zanuttini*
14:00	**Edge Reduction for EVMDDs to Speed Up Analysis of Multi-State Systems** *S. Nagayama, T. Sasao, J. T. Butler, M. A. Thornton, and T. W. Manikas*	**Clones of Pivotally Decomposable Functions** *M. Couceiro and B. Teheux*
14:30	**Belief Network Support via Decision Diagrams** *S. C. Eastwood, S. N. Yanushkevich, and V. P. Shmerko*	**Lazy Clones and Essentially Minimal Groupoids** *H. Machida and T. Waldhauser*
15:00	**Using QMDD in Numerical Methods for Solving Linear Differential Equations via Walsh Functions** *R. S. Stanković and D. M. Miller*	**Some Classes of Centralizing Monoids on a Three-Element Set** *M. Goldstern, H. Machida, and I. G. Rosenberg*
15:30	Coffee/Tea Break	
16:00	Plenary Session and Closing	
	Reed-Muller Workshop Workshop Chair: *D. M. Miller*	

May 21, Thursday	
	Reed-Muller Workshop Workshop Chair: *D. M. Miller*