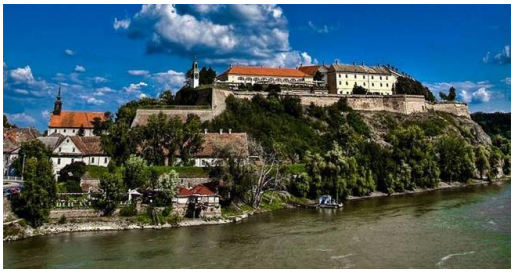
47th IEEE International Symposium on Multiple-Valued Logic

ISMVL 2017

May 22 – 24, 2017, University of Novi Sad, Novi Sad, Serbia

Tentative Program


Sponsored by: IEEE, IEEE Computer Society, TC on Multiple-Valued Logic

May 21, Sunday	
09:15	Workshop on Post-Binary ULSI Systems Workshop Chair: *M. Natsui and H. Nakahara*

May 22, Monday		
09:00	Opening Symposium Chair: *J. Pantović* and Program Chair: *E. Dubrova*	
09:15	**[Keynote Address I]** **An Algorithm for Constraint Satisfaction Problem** *Dmitriy Zhuk (Moscow State University, Russia)*	
10:00	Coffee/Tea Break	
	[Session 1A: Signal Processing & VLSI Design]	**[Session 1B: Algebra & Logic I]**
10:15	**Analog-to-Digital Converters Using not Multi-Level but Multi-Bit Feedback Paths** *T. Waho*	**Phase Semantics for Multilattice Formalism** *N. Kamide*
10:40	**A PAM-4 Eye Diagram Analysis and Its Monitoring Technique for Adaptive Pre-Emphasis for Multi-Valued Data Transmission** *Y. Yuminaka, T. Kitamura, and Y. Iijima*	**Median Based Calculus for Lattice Polynomials and Monotone Boolean Functions** *M. Couceiro, P. Mercuriali, R. Péchoux, and A. Saffidine*
11:05	**Fine-Grain Pipelined Reconfigurable VLSI Architecture Based on Multiple-Valued Multiplexer Logic** *K. Shimabukuro and M. Kameyama*	**Posets of Minors of Functions in Multiple-Valued Logic** *E. Lehtonen and T. Waldhauser*
11:30	**A Novel Ternary Multiplier Based on Ternary CMOS Compact Model** *Y. Kang, J. Kim, S. Kim, S. Shin, E. Jang, J. W. Jeong, K. R. Kim, and S. Kang*	**Extending Ideal Paraconsistent Four-Valued Logic** *N. Kamide*
11:55	Lunch	

May 22, Monday (continued)		
13:30	**[Dedication Talk to the Memory of Ivan Stojmenvić]** **A LifeWell-Spent in the Service of Science** *Dan Simovici (University of Massachusetts Boston, USA)*	
14:15	Coffee/Tea Break	
	[Session 2A: Spectral Techniques]	**[Session 2B: Clone Theory – Special Session –]**
14:30	**On Fixed Points of the Reed-Muller-Fourier Transform** *C. Moraga, R. Stanković, M. Stanković, and Suzana Stojković*	**On the Nonexistence of Minimal Strong Partial Clones** *M. Couceiro, L. Haddad, and K. Schölzel*
14:55	**Some Spectral Invariant Operations for Multiple-Valued Functions with Homogeneous Disjoint Products in the Polynomial Form** *M. Stanković, C. Moraga, and R. Stanković*	**On the Interval of Boolean Strong Partial Clones Containing Only Projections as Total Operations** *M. Couceiro, L. Haddad, V. Lagerqvist, and B. Roy*
15:20	**Properties of the Two-Sided RMF Spectrum of Matrices** *C. Moraga and R. Stanković*	**On an Interval of Slupecki Partial Clones** *L. Haddad and K. Schölzel*
15:45	**Towards the Gibbs Characterization of a Class of Quaternary Bent Functions** *R. Stanković, M. Stanković, J. Astola, and C. Moraga*	**Three Classes of Closed Sets of Monomials** *H. Machida and J. Pantović*
16:10	Coffee/Tea Break	
	[Session 3A: Fuzzy Logic]	**[Session 3B: Design for Security]**
16:25	**Hintikka Style Game Rules for Semi-Fuzzy Quantifiers** *C. Fermüller and M. Hofer*	**Physical Unclonable Functions based on Carbon Nanotube FETs** *M. Moradi, S. Tao, and R. F. Mirzaee*
16:50	**Term Models of Horn Clauses over Rational Pavelka Predicate Logic** *V. Costa and P. Dellunde*	**TVL-TRNG: Sub-Microwatt True Random Number Generator Exploiting Metastability in Ternary Valued Latches** *S. Tao and E. Dubrova*
17:15	**Non-Deterministic Matrices in Action: Expansions, Refinements, and Rexpansions** *A. Avron and Y. Zohar*	**A Systematic Design of Tamper-Resistant Galois-Field Arithmetic Circuits Based on Threshold Implementation with (d + 1) Input Shares** *R. Ueno, N. Homma, and T. Aoki*

May 23, Tuesday		
09:15	**[Keynote Address II]** **Deep Learning for Autonomous Vehicles** *Branislav Kisačanin (Nvidia Corporation, USA)*	
10:00	Coffee/Tea Break	
	[Session 4A: Algorithms & Computational Complexity]	**[Session 4B: Reversible Computing]**
10:15	**Discovery of Multiple-Valued Bent Functions in Galois Field and Reed-Muller-Fourier Domains** *M. Radmanović and R. Stanković*	**Skipping Embedding in the Design of Reversible Circuits** *A. Zulehner and R. Wille*
10:40	**Fast Computation of the Discrete Pascal Transform** *D. Gajić and R. Stanković*	**Exact Synthesis of Ternary Reversible Functions using Ternary Toffoli Gates** *A. Kole, P. M. N. Rani, K. Datta, I. Sengupta, and R. Drechsler*
11:05	**Exploiting Many-Valued Variables in MaxSAT** *J. Argelich, C.-M. Li, and F. Manya*	**Extensions to the Reversible Hardware Description Language SyReC** *Z. Al-Wardi, R. Wille, and R. Drechsler*

May 23, Tuesday (continued)		
	[Session 4A: Algorithms & Computational Complexity]	**[Session 4B: Reversible Computing]**
11:30	**An Exact Optimization Algorithm for Linear Decomposition of Index Generation Functions** *S. Nagayama, T. Sasao, and J. Butler*	**Study of Reversible Ternary Functions with Homogeneous Component Functions** *P. Kerntopf, K. Podlaski, C. Moraga, and R. Stanković*
11:55	**Algebraic and Combinatorial Methods for Reducing the Number of Variables of Partially Defined Discrete Functions** *J. Astola, P. Astola, R. Stanković, and I. Tabus*	
12:20	Lunch	
13:30	Excursion & Banquet	

May 24, Wednesday		
09:15	**[Keynote Address III]** **Index Generation Functions: Minimization Methods** *Tsutomu Sasao (Meiji University, Japan)*	
10:00	Coffee/Tea Break	
	[Session 5A: Quantum & Stochastic Computing]	**[Session 5B: Algebra & Logic II]**
10:15	**Natural Deduction for Connexive Paraconsistent Quantum Logic** *N. Kamide*	**The Groupoid-Based Logic for Lattice Effect Algebras** *I. Chajda, H. Länger, and J. Paseka*
10:40	**Study of GPU Acceleration in Genetic Algorithms for Quantum Circuit Synthesis** *M. Lukac and G. Krylov*	**Centralizing Monoids and the Arity of Witnesses** *H. Machida and I. Rosenberg*
11:05	**On the Fault Tolerance of Stochastic Decoders** *A. Hussein, M. Elmasry, and V. Gaudet*	**Computing Uniform Interpolants in Nilpotent Minimum Logic** *D. Valota*
11:30	**Evaluation of Stochastic Cascaded IIR Filters** *N. Onizawa, S. Koshita, S. Sakamoto, M. Kawamata, and T. Hanyu*	**Nomura Parameters for S-threshold Functions** *I. Prokić and J. Pantović*
11:55	Lunch	
13:30	**[Dedication Talk to the Memory of Bogdan Falkowski]** **In Memoriam Bogdan Falkowski** *Claudio Moraga (Technical University of Dortmund, Germany)*	
14:15	Coffee/Tea Break	
	[Session 6A: Decision Diagrams]	**[Session 6B: Logic & Physical Synthesis]**
14:30	**Error Bounded Exact BDD Minimization in Approximate Computing** *S. Froehlich, D. Grosse, and R. Drechsler*	**Classifying Functions with Exact Synthesis** *W. Haaswijk, E. Testa, M. Soeken, and G. De Micheli*
14:55	**Multi-Valued Decision Diagrams for k-out-of-n Three-State Systems** *M. Kvassay, E. Zaitseva, V. Levashenko, and J. Kostolny*	**OR-Inverter Graphs for the Synthesis of Optical Circuits** *A. Deb, R. Wille, and R. Drechsler*
15:20	**A Random Forest Using a Multi-Valued Decision Diagram on an FPGA** *H. Nakahara, A. Jinguji, S. Sato, and T. Sasao*	**CMOS-Compatible Ternary Device Platform for Physical Synthesis of Multi-Valued Logic Circuits** *S. Shin, E. Jang, J. W. Jeong, and K. R. Kim*
15:45	Coffee/Tea Break	
16:00	Plenary Session & Closing	

May 25, Thursday	
09:15	Reed-Muller 2017 Workshop Workshop Chair: *R. Stanković*