22nd International Workshop on Post-Binary ULSI Systems

May 21, 2013

Toyama International Conference Center, Toyama, Japan

Final Program

Opening Remark: 09:30 - 09:40

Naofumi Homma (*General Co-chair, Tohoku University*)

Invited Talk: 09:40 - 10:40

Ultrahigh-Speed Digital-to-Analog Converters for Multi-Level Optical Transmission Systems

Munehiko Nagatani, Hideyuki Nosaka, ShogoYamanaka, and Koichi Murata (*NTT Photonics Laboratories*)

Break: 10:40 - 10:55

Session 1: 10:55 - 11:45

- *Evaluation of a high-speed data transmission on micro-strip line in VLSI systems*
  Yosuke Iijima (*Oyama National College of Technology*) *and Yasushi Yuminaka* (*Gunma University*)
- *Digital Hardware Implementation of a Fuzzy-Logic-Based Finite-Time Convergence Technique for MOSFET Inverters*
  En-Chih Chang, Hung-Liang Cheng, and Chien-Hsuan Chang (*I-Shou University*)

Lunch Break: 12:00 - 13:30

Session 2: 13:30 – 14:45

- *Optimizing q-Valued Quantum Multiplexers*
  Tahsin Saffat (*Westview High School*) *and Marek Perkowski* (*Portland State University*)
- *Artistic Robots through Interactive Genetic Algorithm with ELO rating system*
  Andy Goetz, Camille Huffman, Kevin Riedl, Mathias Sunardi and Marek Perkowski (*Portland State University*)
- *Methodology to Create Hardware Oracles for Solving Constraint Satisfaction Problems*
  Alan Cheng, Edison Tsai and Marek Perkowski (*Portland State University*)

Break: 14:45 - 15:00

Session 3: 15:00 - 15:50

- *Efficient Specification Method for Model Checking*
  Chikatoshi Yamada (*Okinawa National College of Technology*), *Yasunori Nagata* (*University of the Ryukyus*), *and Michael Miller* (*University of Victoria*)
- *Towards Efficient Evaluation of EM information leakage from cryptographic devices*
  Naofumi Homma, Yu-ichi Hayashi (*Tohoku University*), *Toshihiro Katashita, Yohei Hori* (*AIST*), *and Takafumi Aoki* (*Tohoku University*)

Short Break: 15:50 - 15:55

Short Presentation for Poster Session: 15:55- 16:30

- Poster No. 1: *Voltage-Mode/Current-Mode Hybrid Logic Circuit for a Low-Power Fine-Grain Reconfigurable VLSI*
  Xu Bai and Michitaka Kameyama (*Tohoku University*)
- Poster No. 2: *Logic-in-Memory Architecture for a Multiple-Valued Reconfigurable VLSI Based on Packet Data Transfer Scheme*
  Shintaro Harada, Xu Bai (*Tohoku University*), *Yoshichika Fujioka* (*Hachinohe Institute of Technology*), *and Michitaka Kameyama* (*Tohoku University*)
- Poster No. 3: *Implementation of Wide Band Discrete Wavelet Transform for a Radio Telescope*
  Koushiro Shiihara, Hiroki Nakahara, and Hiroyuki Nakanishi (*Kagoshima University*)
- Poster No. 4: *Multiple-Valued Coding Techniques for Efficient Data Transmission based on Spectral Shaping*
  Yuuki Takada (*Gunma University*), *Yosuke Iijima* (*Oyama National College of Technology*), *and Yasushi Yuminaka* (*Gunma University*)
- Poster No. 5: *A Method of Selecting Radices for Non-binary Successive Approximation A/D Converters*
  Tsutomu Habara and Yukihiro Iguchi (*Meiji University*)
- Poster No. 6: *A 2nd -Order Delta-Sigma Modulator Using Dynamic-Source-Follower Integrator*
  Ryo Matsushiba, Hiroto Kotani, Ryoto Yaguchi, and Takao Waho (*Sophia University*)
- Poster No. 7: *GaAs Nanowire FET-integrated Threshold Logic Circuit*
  Ryota Kuroda and Seiya Kasai (*Hokkaido University*)

Closing: 16:30 - 16:40

Shinobu Nagayama (*General Co-chair, Hiroshima City University*)